

Fig. 1

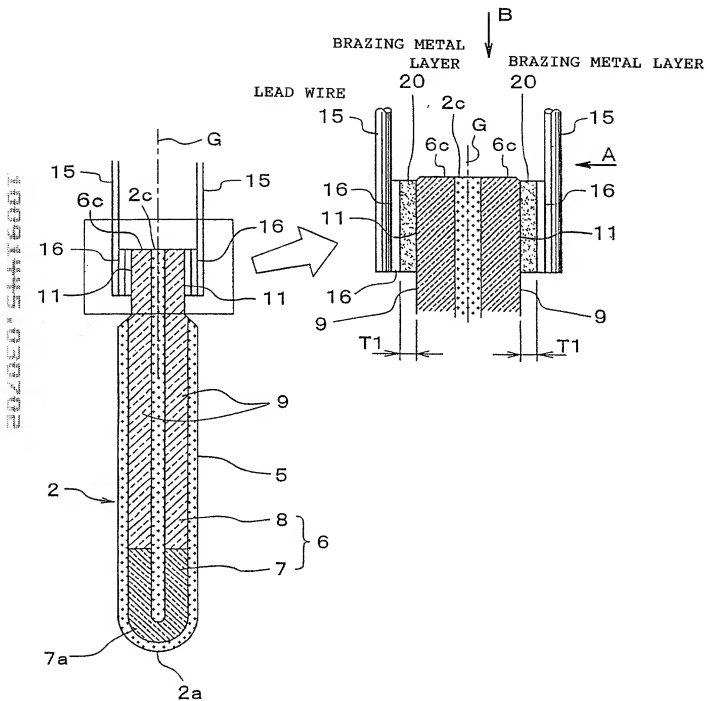


Fig. 2

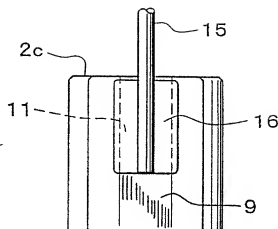


Fig. 3

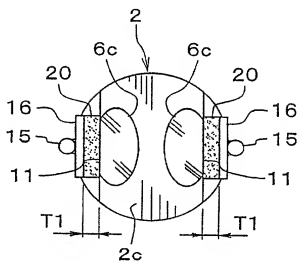


Fig. 1 is a cross-sectional view of a semiconductor device assembly. The assembly includes a central substrate 11 with a top layer 16 and a bottom layer 9. The substrate 11 is divided into regions 20, 6c, and G. Regions 20 are covered by a BRAZING METAL LAYER 22. Lead wires 15 are attached to the top of the substrate. A BUFFER MATERIAL 25 is located below the substrate 11. Arrows T1, T2, and T3 indicate thermal treatment directions, and T indicates a time interval.

FIG. 1 is a cross-sectional view of a semiconductor device. The device consists of a central substrate 2. On the top surface of the substrate 2, there are two circular regions 2c. Between these regions, there is a gap. On the left and right sides of the substrate 2, there are two sets of layers. Each set includes a buffer material 25 at the bottom, followed by a layer 11, a layer 15, and a top layer 16. A brazing metal layer 20 is located between the buffer material 25 and the layer 11. The distance between the centers of the two circular regions 2c is labeled T.

Fig. 6

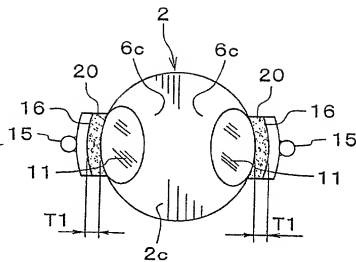


Fig. 7

